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INFORMATION DISCLOSURE CITATION *(Use several sheets if necessary)*	APPLICANT Joerg Vollrath	EXAMINER Not Yet Assigned.
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U. S. PATENT DOCUMENTS

Examiner INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

DM	A	Joerg Vollrath and Randall Rooney, "Pseudo Fail Bit Map Generation for RAMs during Component Test and Burn-In in a Manufacturing Environment," Test Conference, 2001. Proceedings. Int'l, IEEE, pp. 768-775, (Oct. 30 – Nov. 1, 2001).
DM	B	Jorg Vollrath, Ulf Lederer, and Thomas Hladschik, "Compressed Bit Fail Maps for Memory Fail Pattern Classification," European Test Workshop, 2000. Proceedings. IEEE, pp. 125-130, (May 23-26, 2000).
DM	C	U.S. Patent Application No. 09/455,855, filed December 7, 1999, entitled "Efficient Bit Fail Map Compression Strategy".
DM	D	U.S. Patent Application No. 09/931,125, filed August 16, 2001, entitled "Pseudo Fail Bit Map Generation For RAMs During Component Test and Burn-In In A Manufacturing Environment".

EXAMINER Darrell Lacke DATE CONSIDERED 09/15/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line thr ugh citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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